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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,513	04/20/2001	Paul F. Struhsaker	WEST14-00033	2906

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EXAMINER	
PHAN, RAYMOND NGAN	

ART UNIT	PAPER NUMBER
2111	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/839,513	STRUHSAKER ET AL.
	Examiner	Art Unit
	Raymond Phan	2112

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 12-18* is/are rejected.

7)☒ Claim(s) *9-11,19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ ~~Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)~~ Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Notice to Applicant(s)

1. This action is responsive to the following communications: amendment filed on June 1, 2004

2. This application has been examined. Claims 1-20 are pending.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4, 12-14, 18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Barenys et al. (US No. 6,145,036) in view of Khosrowpour (US No. 6,721,817).

In regard to claims 1, 12, Barenys et al. disclose the use in association with a backplane of the item of electronic equipment wherein the backplane comprising a common control bus 220 (i.e. I^2C bus) that can access a first number of device locations, an apparatus 202 capable of allowing the common control bus to access more than one first number of device locations (i.e. address) (see figure 2, col. 3, line 11 through col. 4, line 42).

But Barenys et al. do not specifically disclose the apparatus comprising a complex programmable logic device (i.e. CPLD) on the circuit board within the backplane, wherein the complex programmable logic device is coupled to the common control bus, and wherein the complex programmable logic device is capable of coupling each one of the plurality of device locations on the circuit board card to the common control bus. However Khosrowpour discloses the configuration circuit 250 (i.e. PLD) on the circuit board 150 (OEM circuit) within the backplane, wherein the programmable logic device is coupled to the common control bus, and wherein the complex programmable logic device is capable of coupling each one of the plurality of device locations on the circuit board card to the common control bus (see figure 2, col. 4, line 51 through col. 5, line 23). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Khosrowpour within the system of Barenys et al. because it would allows for better failure isolation and reduce the amount of down-time on the system

In regard to claim 2, Kim et al. disclose wherein the complex programmable logic device controls the access of a device to the common control bus when a device location of the device is coupled to the common control bus (see figure 2, col. 4, line 51 through col. 5, line 23). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Khosrowpour within the system of Barenys et al. because it would allows for better failure isolation and reduce the amount of down-time on the system

In regard to claims 3, 13, Khosrowpour discloses wherein the complex PLD coupled to device location the circuit board card to the common bus

control to allow the common control bus to access a second number of device locations on the circuit board card through the complex PLD (see figure 2, col. 4, line 51 through col. 5, line 23). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Khosrowpour within the system of Barenys et al. because it would allows for better failure isolation and reduce the amount of down-time on the system

In regard to claim 4, 14, Khosrowpour discloses wherein the second number of device locations on the circuit board card that the common control bus can access through the complex PLD is greater than the first number of device locations that the common control bus can otherwise access (see figure 2, col. 4, line 51 through col. 5, line 23). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Khosrowpour within the system of Barenys et al. because it would allows for better failure isolation and reduce the amount of down-time on the system

In regard to claim 18, Barenys et al. disclose the use in association with a backplane of the item of electronic equipment wherein the backplane comprising a common control bus 220 that can access a first number of device locations (i.e. address), an apparatus capable of allowing the common control bus to access more than one first number of device locations (see figure 2, col. 3, line 11 through col. 4, line 42). But Barenys et al. do not disclose the apparatus comprising a complex programmable logic device (i.e. PLD) on the circuit board within the backplane, wherein the complex programmable logic device is coupled to the common control bus, and wherein the complex programmable logic device is capable of coupling each

one of the plurality of device locations on the circuit board card to the common control bus; receiving data in the PLD through the signal bus line; interpreting instructions in the data to allow PLD to control data access to the first device. However Khosrowpour discloses programmable logic device (i.e. PLD) on the circuit board within the backplane, wherein the programmable logic device is coupled to the common control bus, and wherein the complex programmable logic device is capable of coupling each one of the plurality of device locations on the circuit board card to the common control bus (see figure 2, col. 4, line 51 through col. 5, line 23); receiving data in the PLA through the signal bus line (see col. 6, line 43 through col. 7, line 53); interpreting instructions in the data to allow PLA to control data access to the first device (see col. 6, line 43 through col. 7, line 53). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Khosrowpour within the system of Barenys et al. because it would allows for better failure isolation and reduce the amount of down-time on the system

6. Claims 5-8 and 15-17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Barenys et al. in view of Khosrowpour and further in view of Ptasinski et al. (US No. 6,363,437).

In regard to claim 5, Barenys et al. and Khosrowpour teach the claimed subject matter as discussed above except the teaching of a card processor (i.e. controller) on the circuit board card within the back plane, the card processor coupled to the common control bus (see figure 7A, col. 3, lines 47-62). Therefore, it would have been obvious to a person of an

ordinary skill in the art at the time the invention was made to have combined the teachings of Ptasinski et al. within the system of Barenys et al. and Khosrowpour because it would reduce the costs and increase reliability by implementing all functions for the hot plug on a single chip.

In regard to claim 6, Ptasinski et al. disclose wherein the card processor is coupled to the common control bus through the serial clock line (SCL) and through the serial data line (SDL) connection (see figure 7A, col. 3, lines 47-62). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Ptasinski et al. within the system of Barenys et al. and Khosrowpour because it would reduce the costs and increase reliability by implementing all functions for the hot plug on a single chip.

In regard to claims 7, 17, Ptasinski et al. disclose further comprising the EEPROM on the circuit board card coupled to the common control bus; wherein the complex PLD controls the access of EEPROM to the common control bus when the EEPROM is coupled to the common control bus (see figure 7A, col. 3, lines 47-62). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Ptasinski et al. within the system of Barenys et al. and Khosrowpour because it would reduce the costs and increase reliability by implementing all functions for the hot plug on a single chip.

In regard to claim 8, Ptasinski et al. disclose wherein the EEPROM is coupled to the common control bus through the serial clock line (SCL) and through the serial data line (SDL) connection (see figure 7A, col. 3, lines 47-62). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings

of Ptasinski et al. within the system of Barenys et al. and Khosrowpour because it would reduce the costs and increase reliability by implementing all functions for the hot plug on a single chip.

In regard to claim 15, Ptasinski et al. disclose further comprising the step of coupling the card processor on the circuit board card within the back plane to the common bus; providing clock signals to the card processor from the serial clock line coupled to the common data bus; reading data from the card processor on the serial data line coupled to the common data bus; and writing data to the card processor from the serial data line (see figure 7A, col. 3, lines 47-62). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Ptasinski et al. within the system of Barenys et al. and Khosrowpour because it would reduce the costs and increase reliability by implementing all functions for the hot plug on a single chip.

In regard to claim 16, Ptasinski et al. disclose further comprising the step of coupling the EEPROM on the circuit board card within the back plane to the common bus; providing clock signals to the EEPROM from the serial clock line coupled to the common data bus; reading data from the EEPROM on the serial data line coupled to the common data bus; and writing data to the card processor from the serial data line (see figure 7A, col. 3, lines 47-62). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Ptasinski et al. within the system of Barenys et al. and Khosrowpour because it would reduce the costs and increase reliability by implementing all functions for the hot plug on a single chip.

Allowable Subject Matter

7. Claims 9-11, 19-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments, see pages 13-24, filed on June 1, 2004, with respect to the rejectionsof claims 1-20 under 35USC103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Barenys et al. and Khosrowpour .

Conclusion

9 Claims 1-8 and 12-18 are rejected. Claims 9-11 and 19-20 are objected.

10. The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure.

Anderson et al. (US No. 6,629,172) disclose a multi-chip addressing for the I2C bus

Wachel (US No. 6,675,254) discloses a system and method for mid-plane interconnect using switched technology.

Bouchier et al. (US No. 6,725,317) disclose a system and method for managing a computer system having a plurality of partitions.

Strugger et al. (US No. 4,882,702) disclose a programmable controller with I/O expansion module located in one of the I/O module positions for communication with outside I/O modules.

Tomlinson et al. (US No. 6,735,706) disclose a programmable power management system and method.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (703) 306-2756. The examiner can normally be reached on Monday-Friday from 6:30AM- 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Primary, Paul Myers can be reached on (703) 305-9656 or via e-mail addressed to paul.myers@uspto.gov. The fax phone number for this Group is (703) 872-9306.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [**raymond.phan@uspto.gov**].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Paul R. Myers

PAUL R. MYERS
PRIMARY EXAMINER

Raymond Phan
8/31/04